WHAT IS CLAIMED IS:

1. A liquid crystal display device, comprising:

a line memory for dividing a data for at least one line inputted from the exterior thereof into a plurality of groups to store the divided data therein and for outputting the data at a desired unit from each of the groups;

a driving circuit including n driver integrated circuits(wherein n is an integer) that are connected to the line memory and a liquid crystal display panel to drive the liquid crystal display panel in response to the data outputted from the line memory; and

a timing controller, being connected to the line memory and the driving circuit, for receiving a data clock inputted from the exterior thereof to output the data from the plurality of groups of said line memory to the driving circuit every period of the data clock in response to a time corresponding to the number of said groups.

2. The liquid crystal display device as claimed in claim 1, wherein the plurality of groups consist of a first group and a second group including data inputted to 1st to (n/2)th driver integrated circuits and to ((n+1)/2)th to nth driver integrated circuits, respectively.

3. The liquid crystal display device as claimed in claim 2, wherein the timing controller generates an inverted data clock having a phase contrary to the input data clock and outputs a data from the first group of the line memory in response to the data clock while outputting a

data from the second memory group of the line memory in response to the inverted data clock, thereby outputting the data in the first group and the data in the second group to the driving circuit at a different time during each period of the data clock.

4. The liquid crystal display device as claimed in claim 1, wherein the plurality of groups consist of a first group and a second group including data inputted to odd-numbered driver integrated circuits and even-numbered driver integrated circuits in the driving circuit connected to the liquid crystal display panel, respectively.

5. The liquid crystal display device as claimed in claim 4, wherein the timing controller generates an inverted data clock having a phase contrary to the input data clock and outputs a data from the first group of the line memory in response to the data clock while outputting a data from the second memory group of the line memory in response to the inverted data clock, thereby outputting the data in the first group and the data in the second group to the driving circuit at a different time during each period of the data clock.

6. The liquid crystal display device as claimed in claim 1, wherein the plurality of groups consist of a first group and a second group including data inputted to upper driver integrated circuits and lower driver integrated circuits in the driving circuit connected to the upper and lower sides of the liquid crystal display panel, respectively.

7. The liquid crystal display device as claimed in claim 6, wherein the timing controller generates an inverted data clock having a phase contrary to the input data clock and outputs a data from the first group of the line memory in response to the data clock while outputting a data from the second memory group of the line memory in response to the inverted data clock, thereby outputting the data in the first group and the data in the second group to the driving circuit at a different time during each period of the data clock.

8. A liquid crystal display device, comprising:

a line memory for dividing a data for at least one line inputted from the exterior thereof into a plurality of groups to store the divided data therein and for outputting the data at a desired unit from each of the groups;

a driving circuit including n driver integrated circuits(wherein n is an integer) that are connected to the line memory and a liquid crystal display panel to drive the liquid crystal display panel in response to the data outputted from the line memory; and

a timing controller, being connected to the line memory and the driving circuit, for receiving a data clock inputted from the exterior thereof to generate a first data clock by frequency-dividing the data clock at a frequency-division ratio corresponding to the number of said divided groups, and for outputting the data in each of the groups to the driving circuit during each period of the first data clock.

9. The liquid crystal display device as claimed in claim 8, wherein the plurality of groups consist of a first group and a second group including data to be displayed on the liquid crystal display panel connected to 1st to (n/2)th driver integrated circuits and to ((n+1)/2)th to nth driver integrated circuits, respectively.

10. The liquid crystal display device as claimed in claim 9, wherein the timing controller generates an inverted data clock having a phase contrary to the frequency-divided data clock and outputs a data from the first group of the line memory in response to the frequency-divided data clock while outputting a data from the second memory group of the line memory in response to the inverted data clock, thereby outputting the data in the first group and the data in the second group to the driving circuit at a different time during each period of the data clock.

11. The liquid crystal display device as claimed in claim 8, wherein the plurality of groups consist of a first group and a second group including data inputted to odd-numbered driver integrated circuits and even-numbered driver integrated circuits in the driving circuit connected to the liquid crystal display panel, respectively.

12. The liquid crystal display device as claimed in claim 4, wherein the timing controller generates an inverted data clock having a phase contrary to the input data clock and outputs a data from the first group of the line memory in response to the data clock while outputting a data from the second memory group of the line memory in response to the inverted data clock, thereby outputting the data in the first group and the data in the second group to the driving circuit at a different time during each period of the data clock.

13. A liquid crystal display device, comprising:

a line memory for receiving two pixel data unit sequentially from the exterior thereof and dividing the data for at least one line into a plurality of groups to store the divided data therein and for outputting the two pixel data unit from each of the groups;

a driving circuit including n driver integrated circuits(wherein n is an integer) that are connected to the line memory and a liquid crystal display panel to drive the liquid crystal display panel in response to the data outputted from the line memory; and

a timing controller, being connected to the line memory and the driving circuit, for receiving a data clock inputted from the exterior thereof to generate a first data clock by frequency-dividing the data clock at a frequency-division ratio corresponding to the number of said divided groups, and for outputting the two pixel data in each of the groups to the driving circuit during each period of the first data clock.

14. The liquid crystal display device as claimed in claim 13, wherein the plurality of groups consist of a first group and a second group including data to be displayed on two divisional area divided into the left and right sides of the liquid crystal display panel, respectively.

15. The liquid crystal display device as claimed in claim 14, wherein the timing controller generates a second data clock having a phase contrary to the first data clock and outputs two pixel data from the first group of the line memory in response to the first data clock while outputting two pixel data from the second memory group of the line memory in response to the second data clock, thereby supplying the two pixel data unit from the first group and the second group of the line memory to the driving circuit at a different time interval during each period of the data clock.

16. The liquid crystal display device as claimed in claim 13, wherein the plurality of groups consist of a first group and a second group including data inputted to odd-numbered driver integrated circuits and even-numbered driver integrated circuits in the driving circuit connected to the liquid crystal display panel, respectively.

17. The liquid crystal display device as claimed in claim 16, wherein the timing controller generates a second data clock having a phase contrary to the first data clock and outputs two pixel data from the first group of the line memory in response to the first data clock while

outputting two pixel data from the second memory group of the line memory in response to the second data clock, thereby supplying the two pixel data unit from the first group and the second group of the line memory to the driving circuit at a different time interval during each period of the data clock.

18. A liquid crystal display device, comprising:

a latch circuit for latching and outputting two pixel unit inputted from the exterior thereof;

a driving circuit including n driver integrated circuits(wherein n is an integer) that are connected to the latch circuit and a liquid crystal display panel to drive the liquid crystal display panel in response to the data outputted from the latch; and

a timing controller, being connected to the latch circuit and the driving circuit, for receiving a data clock inputted from the exterior thereof to output each one pixel data to the driving circuit at a desired time interval during one period of the data clock.

19. The liquid crystal display device as claimed in claim 18, wherein the timing controller generates an inverted data clock having a phase contrary to the input data clock and outputs odd pixel data from the latch circuit in response to the data clock while outputting even pixel data from the latch circuit in response to the inverted data clock, thereby supplying the odd and even data from the latch circuit to the driving circuit at a desired time interval during

each period of the data clock.

20. A method of driving a liquid crystal display device, comprising:

a data storage step of dividing and storing an input data for at least one line a plurality of groups;

a data clock generating step of frequency-dividing an input first data clock at a frequency-division ratio corresponding to the number of said divided groups to generate a second data clock;

a data outputting step of outputting a desired data unit from each of said groups at a different time during one period of the second data clock; and

a displaying step of latching the output data for one line unit to drive a liquid crystal display panel in response to the latched data.

21. The method as claimed in claim 20, wherein the data storage step includes sequentially receiving at least two pixel data to divide and store the data for one line into two groups; the frequency division ratio at the data clock generating step is two; and the two groups at the data storage step individually output the two pixel data at a desired time difference during one period of the second data clock.